08/675217

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO. 19516/159

#11 08-21-96

In re Patent Application of

Ryan FEEMSTER et al.

Serial No. _____ Group Art Unit: 2315

Continuation of: 08/113,299

Filed: Herewith Examiner:

For: DEVICE AND METHOD FOR INTERPROCESSOR COMMUNICATION USING MAILBOXES OWNED BY PROCESSOR DEVICES

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.56

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Submitted herewith on Form PTO-1449 is a listing of documents known to Applicants in order to comply with Applicants duty of disclosure pursuant to 37 CFR 1.56. A copy of each listed document is being submitted to comply with the provisions of 37 CFR 1.97 and 1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicants not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a prima facie prior art reference against the claims of the present application.

CONCISE EXPLANATION OF
RELEVANCE OF EACH DOCUMENT

The Hasegawa article discloses a digital servo controller for a disc drive. The Robla article discloses a real time multi-processor system for controlling robots using an interchange message system/manager of interruptions. The IBM Technical Bulletin discloses dual signal processors.

EU O 156 921 discloses a numerical control apparatus for the main processor and several subsidiary processors for high speed data transfer. UK 2 256 290 discloses a servomotor control system with several servo controllers. EU O 218 036 discloses a control circuit employing multiplexing and impedance matching for servo drives.

The Al-Mouhamed article concerns a multiple module architecture including a tightly coupled set of processors. The Kircanski article discloses a robot control system with three parallel processor boards. The Kametani article concerns industrial robots with a distributed higher article architecture.

U.S. Patent 4,873,476 concerns a robot control apparatus with servo CPU's. U.S. Patent No. 5,187,796 discloses a vector co-processing systems with register-to-register architecture. U.S. Patent No. 4,970,447 discloses a software servo control apparatus capable of changing servo control variable constants. U.S. Patent No. 4,760,521 concerns an arbitration system with multiple processors and a local memory associated with each processor.

U.S. Patent No. 4,965,717 concerns a computer system employing multiple identical CPU's executing the same instruction stream. U.S. Patent No. 5,072,373 concerns a data processing system including a series of processing nodes provided with their own data stores. U.S. Patent No. 5,161,209 concerns a drum servo circuit

controlled by a pair of micro-processors.

U.S. Patent No. 5,193,197 concerns a data processing system with resource units shared by several processing units, and an arbitration unit. U.S. Patent No. 5,319,753 concerns a bi-directional interrupt technique and mechanism for handling programmable lengthy interrupt messages between two devices. U.S. Patent No. 5,146,596 concerns arbitration and control circuitry for monitoring two processors sharing a system bus.

U.S. Patent No. 5,038,276 concerns a data processing system with a dual arbiter for controlling access to a system bus. U.S. Patent No. 5,142,689 concerns a multiple processor network with a centrally synchronized bus.

U.S. Patent No. 5,136,714 concerns an inter-processor interrupt mechanism in a shared memory multi-processor system. U.S. Patent No. 5,127,089 concerns a data processing system including two processors coupled via the communication bus and the bus arbiter. U.S. Patent No. 5,202,966 concerns a centralized bus arbitration circuit allowing processors access to a bus.

U.S. Patent No. 4,879,642 concerns a servo loop processor used with a main processing unit. U.S. Patent No. 5,271,020 concerns a method of handling invalid data transmitted from one agent to another.

The listed documents are being submitted in compliance with 37 C.F.R. §1.97(b), within three (3) months of the filing date.

Applicants respectfully request that the listed documents be considered by the Examiner and formally be made of record in the present application and that an

initialled copy of Form PTO-1449 be returned in accordance with MPEP §609.

Respectfully submitted,

July 3, 1996

Brian J. McNamara
Reg. No. 36,880

FOLEY & LARDNER
3000 K Street, N.W.
Suite 500
Washington, D.C. 20007-5109
Tel: (202) 672-5300